2013-1192
(Reexamination Nos. 95/000,166 and 95/001,122)

United States Court of Appeals for the Federal Circuit

RAMBUS, INC.,

Appellant,

v.

MICRON TECHNOLOGY, INC.,

Appellee.

Appeal from the United States Patent and Trademark Office, Patent Trial and Appeal Board.

BRIEF OF APPELLEE MICRON TECHNOLOGY, INC.

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JULY 19, 2013

CERTIFICATE OF INTEREST

Counsel for appellee Micron Technology, Inc. certifies the following:

1. The full name of every party or amicus represented by me is:

Micron Technology, Inc.

2. The name of the real party in interest (if the party named in the caption is not the real party in interest) represented by me is:

Micron Technology, Inc.

3. All parent corporations and any publicly held companies that own 10 percent or more of the stock of the party or amicus curiae represented by me are:

None

4. The names of all law firms and the partners or associates that appeared for the party or amicus now represented by me in the trial court or agency or are expected to appear in this court are:

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TABLE OF ABBREVIATIONS

’916 Patent	Rambus’s U.S. Patent No. 6,426,916
’898 application	Application No. 07/510,898, the original parent application to which the ‘916 Patent claims priority
ACP	Action Closing Prosecution
Bennett	U.S. Patent No. 4,734,909, cited by the Board
Board	Board of Patent Appeals and Interferences (now, Patent Trials and Appeals Board)
DRAM	Dynamic Random Access Memory
JEDEC	Joint Electron Device Engineering Council (JEDEC) Standard No. 21-C, Revision 9, published 1999, cited by Micron in its reexamination request
Micron	Micron Technology, Inc., Third Party Requester
Park	U.S. Patent No. 5,590,086, cited by Micron in its reexamination request
PTO	United States Patent and Trademark Office
Rambus	Rambus, Inc., Patent Owner of the ’916 Patent
RAN	Right of Appeal Notice
Samsung	Samsung Electronics Co., Ltd., Third Party Requester
VBI	Versatile Bus Interface
VLSI	Very large scale integrated
VLSIC	Very large scale integrated circuit
A__	Page in Joint Appendix
A__(xx:yy-zz)	Joint Appendix page where xx represents a column number of a patent, yy represents the initial line of cited text and zz represents the ending line of cited text

STATEMENT OF RELATED CASES

Micron is unaware of any other appeals or petitions taken in this reexamination proceeding. There are, however, a number of different matters pending in this Court and other courts that involve U.S. Patent No. 6,426,916 ("the '916 Patent").

1. The following pending cases involve the '916 patent.

    a. *Rambus Inc. v. LSI Corp.*, No. 3:10-cv-05446-RS (N.D. Cal.) (Seeborg, J.).

    b. *Rambus Inc. v. Micron Technology Inc.*, No. 5:06-cv-00244-RMW (N.D. Cal.) (Whyte, J.).

    c. *Rambus Inc. v. STMicroElectronics, N.V.*, No. 3:10-cv-05437-RS (N.D. Cal.) (Seeborg, J.).

2. The following pending cases do not involve the '916 Patent but involve patents that, like the '916 Patent, descend from Application No. 07/510,898 ("the '898 application").

    a. *Rambus, Inc. v. Micron Technology, Inc.*, No. 2013-1087 (Fed. Cir.). This case is currently pending before the Federal Circuit.

    b. *Rambus, Inc. v. Micron Technology, Inc.*, No. 2013-1224 (Fed. Cir.). This case is currently pending before the Federal Circuit.

    c. *Rambus, Inc. v. Micron Technology, Inc.*, No. 2013-1228 (Fed. Cir.). This case is currently pending before the Federal Circuit.

    d. *Rambus, Inc. v. Micron Technology, Inc.*, No. 2013-1339 (Fed. Cir.). This case is currently pending before the Federal Circuit.

    e. *Micron Technology v. Rambus Inc.*, No. 1:00-cv-00792-SLR (D. Del.) (Robinson, J.). This case is on remand from Appeal No. 2009-1263, 645 F.3d 1311 (Fed. Cir. 2011). Rambus has filed an appeal with the

Federal Circuit from the judgment of the district court entered on February 25, 2013.

f. *In re Rambus Inc.*, No. 2011-1247 (Fed. Cir. decided Aug. 15, 2012).

g. *Rambus, Inc. v. Kappos*, No. 2012-1634 (Fed. Cir.) (argued July 11, 2013).

I. STATEMENT OF THE ISSUES

1. Whether substantial evidence supports the Board's conclusion that claims 26 and 28 are anticipated by Bennett where the Board found that at least one embodiment of Bennett's configuration register discloses "a register which stores a value that is representative of an amount of time to transpire after which the memory device outputs the first amount of data," as recited in claims 26 and 28 of the '916 Patent.

II. STATEMENT OF THE CASE

In this case, Micron and Samsung each submitted a request for *inter partes* reexamination of claims 26 and 28 of the '916 Patent. The PTO subsequently merged the two proceedings into a single proceeding.

In the Office Action of March 20, 2009, the examiner initially rejected claims 26 and 28 as anticipated by Bennett. Subsequently, the examiner withdrew the rejections. Micron then appealed the examiner's allowance of claims 26 and 28 to the Board.

In its Decision, the Board determined that the examiner erred in withdrawing the rejection of claims 26 and 28 of the '916 Patent and held that claims 26 and 28 are anticipated by Bennett. In particular, the Board found that the examiner erred by not determining that Bennett discloses a memory device that stores "a value that is representative of an amount of time to transpire after which the memory device

outputs the first amount of data" as recited in claim 26 of the '916 Patent. (A13.) Rambus now appeals the Board's decision that claims 26 and 28 of the '916 Patent are anticipated by Bennett.

In its appeal brief to this Court, Rambus argues that the contested limitation of claim 26 is a "key" point of novelty in allowing memory transactions to be interleaved (i.e., a second transaction can use the bus before a first transaction is completed). (Rambus's Br. at 2-3; *see* A152(7:13-15).) Yet, Rambus fails to even acknowledge that the ability to interleave transactions is one of the core objects of Bennett. (A1329(19:28-33) ("A fifth class of objects of the present invention is to provide a bused digital communication scheme and apparatus wherein communication activities may be selectably configurably pipelined (time overlapped)").) An example of Bennett's interleaved pipelined operations on a bus is shown in Figure 30, where the clock cycles between the beginning of transaction 1 and its completion are used for other transactions (i.e., two outstanding requests are sent onto the bus after transaction 1 begins but before it is completed). (A1362(85:5-6) (explaining that Figure 30 shows "three pipelined transactions"); *see also* A16.)

Moreover, Rambus does not contest that configuring Bennett's wait lines to be either dedicated or multiplexed has the same functional result as the delay time recited in claim 26, namely that the output from a memory device can be

configured to be delayed a finite number of clock cycles. (Rambus's Br. at 40.) As explained in more detail below, what Rambus refers to in its brief as a "tangential[]" effect is actually a known 1 clock cycle delay.

Instead, Rambus tries to distinguish Bennett on a legally untenable position, namely that every single configuration of Bennett must read on the claim under every circumstance in order to anticipate. Rambus does not cite to any legal support for that new theory. Nor could Rambus do so, because that theory contravenes well settled case law holding that a claim is anticipated so long as a single embodiment of a prior art reference reads on the claim. *ArthroCare Corp. v. Smith & Nephew Inc.*, 406 F.3d 1365, 1372 (Fed. Cir. 2005).

Furthermore, underlying the premise of Rambus's argument is that every embodiment of Bennett must output data in the exact same way in order to anticipate. If this were true, it would result in the absurd conclusion that Bennett's expansive discussion of its interconnect system, with numerous different embodiments, would provide virtually no anticipatory disclosure because it is highly configurable.

Rambus does not dispute that the change in a single configuration parameter shown in Bennett Figures 25a and 25b results in adding an additional one clock cycle delay that transpires before data is output. (Rambus's Br. at 6.) Yet, Rambus contends that these figures should not be considered on the grounds that they

purportedly are simplified generic transactions rather than actual memory transactions. (Rambus's Br. at 6-7.) Rambus's position, however, is undercut by the factual findings of both the Board and the District Court in California, both of which found that Figures 25a and 25b represent transactions of a "memory device." (A16 (holding "Figures 25a-h represent generic slave devices and hence encompass memory devices"); A10022 (District Court referring to Figures 25a and 25b as representing a "memory device").)

Rambus directs much of its brief to the arbitration protocol illustrated in Figure 36 of Bennett, which Rambus alleges shows an actual memory transaction. (Rambus's Br. at 7-8.) But Rambus's argument is irrelevant, because the Board's rejection relied on embodiments of Bennett that either did not use an arbitration protocol or won the arbitration on the first attempt. (A19.) Even Rambus acknowledges that at best the arbitration protocol means that "a read request *may* be delayed for an indefinite period of time." (Rambus's Br. 31) (emphasis added and omitted).) Conversely, Rambus admits that in some circumstances the delay would be definite even with an arbitration protocol, and thus claims 26 and 28 would be anticipated.

Finally, as noted by the Board, Rambus's claims are not limited to a method of using a memory device without arbitration. (A19.) Claim 26 when viewed in light of the specification at most only requires a minimum amount of time to

transpire before the memory device outputs data, but does not preclude additional delay caused by other circumstances such as arbitration.

Therefore, the Board's decision should be upheld on multiple grounds. First, Rambus fails to rebut the actual rejection relied on by the Board and instead attacks other embodiments in Bennett. Second, the unsuccessful arbitration depicted in Figure 36 does not override the other disclosure in Bennett, which shows the claimed delay in embodiments where the arbitration protocol is not used or when arbitration is won on the first try. Third, even if Bennett did require repeated arbitration attempts, the claim as properly construed does not preclude such additional delay before outputting data.

III. STATEMENT OF THE FACTS

A. Claims 26 and 28

Claims 26 and 28 are reproduced below with emphasis on limitations at issue in Rambus's Appeal:

> 26. A synchronous semiconductor memory device having at least one memory section including a plurality of memory cells, the memory device comprising:
>
> clock receiver circuitry to receive an external clock signal;
>
> first input receiver circuitry to sample block size information synchronously with respect to the external clock signal, wherein the block size information is representative of an amount of data to be output by the memory device *in response to a first operation code*;

> *a register which stores a value that is representative of an amount of time to transpire after which the memory device outputs the first amount of data*; and
>
> a plurality of output drivers to output the amount of data *in response to the first operation code and after the amount of time transpires*.
>
> (A161-62(26:55-27:3)(emphasis added).)
>
> 28. The memory device of claim 26 wherein in response to a second operation code, the value is stored in the register.
>
> (A162(27:7-8).)

B. Overview of the Prior Art

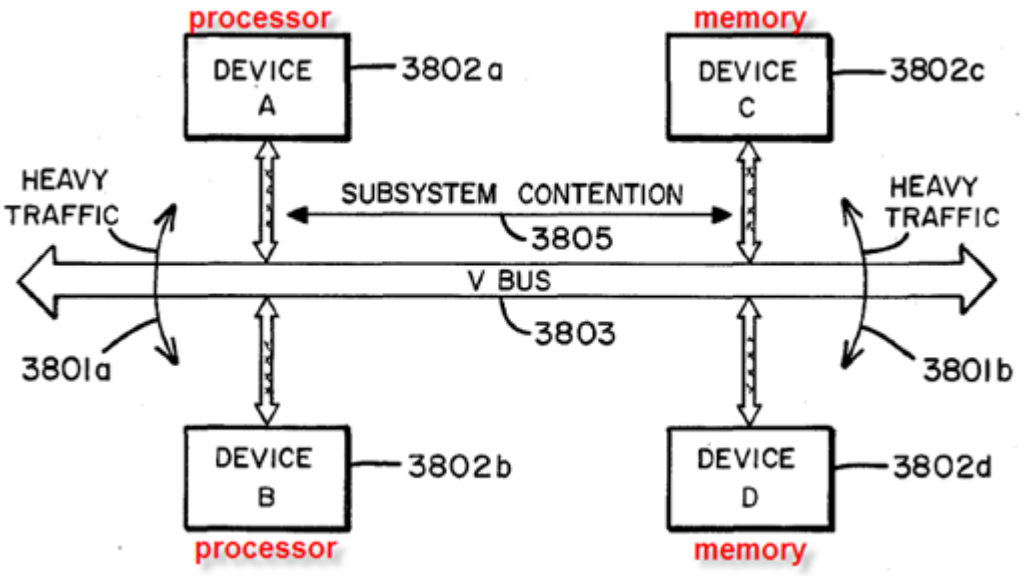
1. Bennett

Bennett describes a highly versatile interconnection scheme to provide high performance, economical resources, and flexible configuration that was designed to become the standard interface for a "myriad [of] devices." (A1325(12:14-25).) Of particular relevance to this appeal, Bennett describes the interconnection of VLSIC "User" devices over a Versatile Bus. (A1325(12:28-32); A1337(35:59-61).) Bennett states that User device can be "a central processor or a memory or whatever." (A1339(40:52-55); A1337(35:59-62).)

"Each Versatile Bus Interface Logics services a User as well as communicating across the Versatile Bus with other Versatile Bus Interface Logics. Therefore, an interface is presented to the User, which may be on a separate chip or, as is more common, will be on the same physical substrate upon which the Versatile Bus logics are implemented in VLSIC." (A1344(50:7-17); A1337(36:19-

25).) In addition, Bennett employs a synchronous protocol over the Versatile Bus to interconnect the Users. (A1352-53(66:9-67:18); A10(¶B7).)

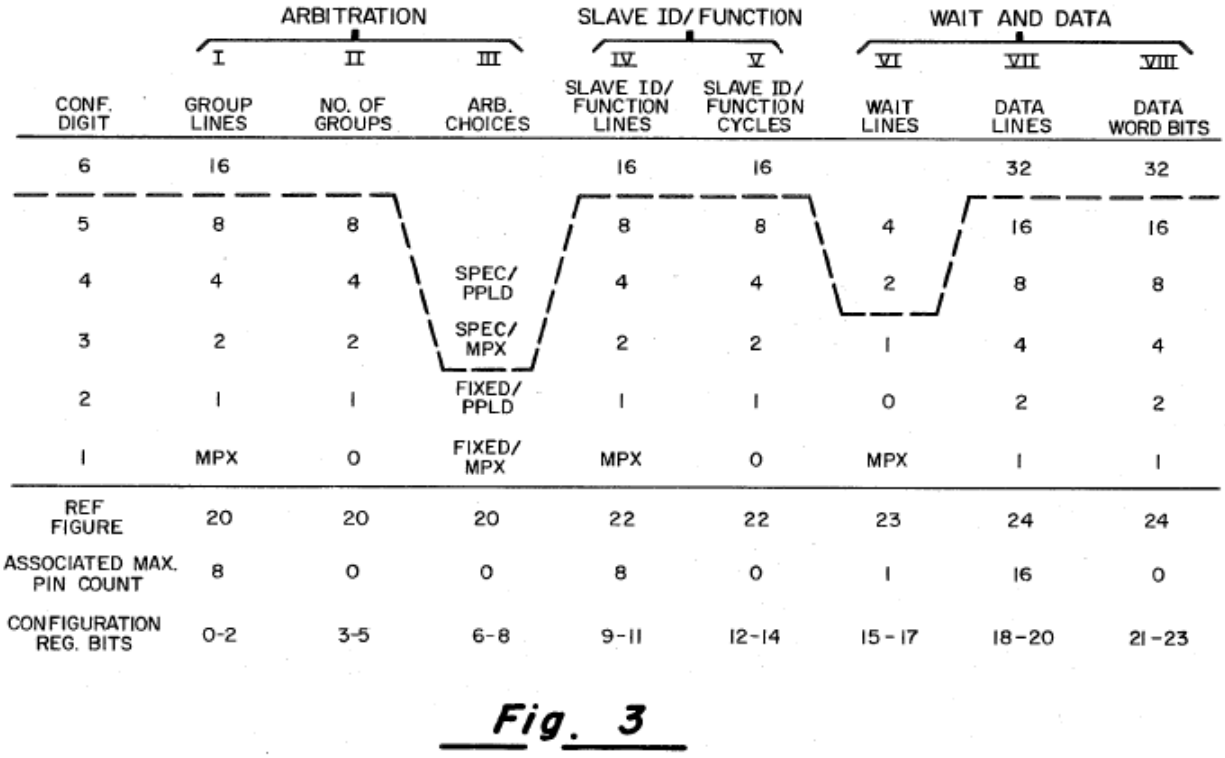
As an example of how memory is accessed, Bennett discloses Figure 38 where "device A and device B are processors that predominantly respectively reference memories device C and device D" over the synchronous Versatile Bus. (A1368(97:7-10) (internal numbering omitted).)



Bennett Figure 38 (A1090) (annotated)

The versatility of Bennett's interface is provided by programming a configuration register within the interface, which instructs the interface to operate according to the selected configuration values. (A1068.) Each User device contains a configuration register that can be programmed. (A1328(17:9-19); A1068.) Each configuration register has eight configuration parameter values, stored in the configuration register as configuration parameters I through VIII. (A1327(15:33-

35); A8(¶B5) (citing A1362(86:31-32).) Among other things, these values control how and when information will be sent between devices on the Versatile Bus. (A1611 (referencing A1362(85:49-86:41)).)



	ARBITRATION			SLAVE ID/FUNCTION		WAIT AND DATA		
	I	II	III	IV	V	VI	VII	VIII
CONF. DIGIT	GROUP LINES	NO. OF GROUPS	ARB. CHOICES	SLAVE ID/ FUNCTION LINES	SLAVE ID/ FUNCTION CYCLES	WAIT LINES	DATA LINES	DATA WORD BITS
6	16			16	16		32	32
5	8	8		8	8	4	16	16
4	4	4	SPEC/ PPLD	4	4	2	8	8
3	2	2	SPEC/ MPX	2	2	1	4	4
2	1	1	FIXED/ PPLD	1	1	0	2	2
1	MPX	0	FIXED/ MPX	MPX	0	MPX	1	1
REF FIGURE	20	20	20	22	22	23	24	24
ASSOCIATED MAX. PIN COUNT	8	0	0	8	0	1	16	0
CONFIGURATION REG. BITS	0-2	3-5	6-8	9-11	12-14	15-17	18-20	21-23

Fig. 3

Bennett Figure 3 (A1068)

For this appeal, the main issues center on parameter VI entitled "Wait Lines." This parameter controls how many bus lines will be exclusively dedicated to transmitting Wait signal information, with configuration values 3 and 1 being most important to this appeal.[1] (A1360(81:63-67).) A configuration value of 3

[1] Wait is a signal sent by a slave device (*e.g.*, a memory device) to the master that indicates whether the slave device is able to accept data in the transaction. The Wait signal gives an indication of whether, or how long it will be before, the data transfer could successfully occur. (A1357(75:54-76:30).)

provides one pin dedicated for the Wait signal while a configuration value of 1 provides that the Wait signal and Data will be multiplexed on the same pin (*i.e.*, Wait and Data share the same pin). The primary distinction between these two options is that when Wait and Data are multiplexed on the same pin, the transmission of Data is delayed because the pin must first be used to send the Wait signal.

Bennett provides numerous examples illustrating the timing of transactions that occur across the Versatile Bus in the various configurations. One of the first in-depth examples is provided in Figures 25a-h. (A1361-63(84:65-87:56).) This set of figures describes a configuration in which each action takes only one clock cycle and helps the reader understand the basics of how the configuration parameters affect the timing of transactions. (A1361-63(84:65-87:56).)

In one example, reproduced below, Bennett discloses for Figure 25a that the configuration register stores the value 122121 as parameters I through VI. (A1362(85:49-86:41).) This configuration value results in a transaction cycle time of 4 clock cycles. (A1362(85:49-86:41).) In Figure 25b, the configuration register stores the value 122123 as parameters I through VI. This configuration – which is the same as Figure 25a except parameter VI is changed from a "1" to a "3" – results in a transaction cycle time of 3 clock cycles. (A1362(85:49-86:41).)

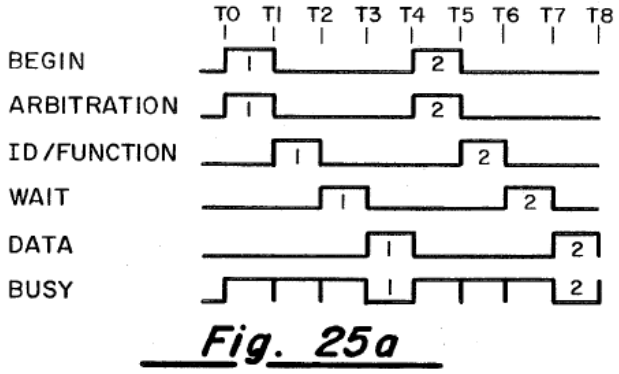


Fig. 25a

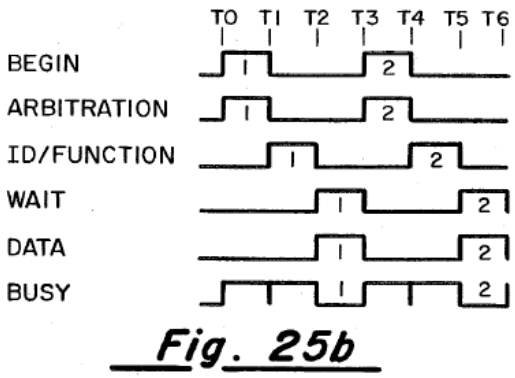


Fig. 25b

[Parameters I-VI: 122121] [Parameters I-VI: 122123]

Bennett FIGs. 25a-b (A1079)

As seen in the figures and described in Bennett, the change of parameter VI from 1 to 3 results in a "reduction in total transaction times from 4 clock cycles to 3 clock cycles." (A1362(86:31-41).) Conversely, the change of parameter VI from 3 to 1 inserts an additional clock cycle between the operation code and the output of data that results in a one clock cycle delay in outputting data.

Therefore, Bennett discloses a configurable register on the User memory device. The configurable register stores configuration parameters that include parameter VI which can be configured to include or not an extra clock cycle of delay before the transmission of data.

2. JEDEC

JEDEC provides a standard according to which compliant controllers and synchronous memory devices must operate. (A10038-A10134.) The standard includes pinouts as well as functional requirements and timing diagrams for

synchronous DRAMs. Timing diagrams show an external clock signal, CK. (A10151.) Control signals CAS, RAS, WE, etc., are used to instruct the memory device to perform certain operations such as Read, Write, Read with Auto Precharge, and Write with Auto Precharge. (*See* A10140 at Table 3.11.5.1-1.) JEDEC discloses a register which stores a value that is representative of an amount of time to transpire after which the memory device outputs the first amount of data. (A10037-A10134; A10153; A10158.)

JEDEC was published in 1999 and was presented as anticipatory art during the reexamination proceeding. Though JEDEC was published after the alleged priority date of the ’916 Patent, Micron argued, on appeal to the Board, that JEDEC must constitute prior art because claims 26 and 28 are not entitled to an effective filing date earlier than the February 27, 2001 filing date of the ’916 Patent. (A1617-1629.)

3. Park

Park describes a “synchronous dynamic random access memory which is capable of accessing data in a memory cell array disposed therein in synchronism with a system clock from an external system such as a central processing unit (CPU).” (A10388(1:9-14).) Figures 5a and 5b of Park disclose activate, read, write, precharge, and refresh operations and show a command that is sampled synchronously with respect to external clock CLK. (A10227(FIGs. 5a-b).) Park

discloses a register which stores a value that is representative of an amount of time to transpire after which the memory device outputs the first amount of data. (A10289(4:59-61); A10290(5:1-2); A10293(11:22-26); A10306(38:9-12); A10243; A10246; A10282.)

Park was filed on December 29, 1995 and was issued on December 31, 1996. Though Park was filed after the alleged priority date of the '916 Patent, Micron argued, on appeal to the Board, that Park must constitute prior art because claims 26 and 28 are not entitled to an effective filing date earlier than the February 27, 2001 filing date of the '916 Patent. (A1617-1629.)

C. Background of the Technology at Issue

1. Dynamic Random Access Memory

Much of the discussion provided in Rambus's brief pertaining to the background of the technology addresses synchronous DRAMs. (Rambus's Br. at 10-13.) However, the claims are not limited to DRAMs, as claims 26 and 28 simply recite "a synchronous semiconductor memory device." Because the claims are not limited to DRAM devices, Rambus's attempt to distinguish Bennett from a DRAM device rather than the claimed "memory device" is irrelevant.

In addition, Rambus asserts that "[p]rior to 1990…, conventional DRAMs operated asynchronously, *i.e.*, without being synchronized with an external clock signal." (Rambus's Br. at 11 (citing A150(3:9-15).) However, synchronous

DRAMs were known at least as early as 1972. (*See* A10311.) In particular, the Intel 4002 was a RAM that was controlled by two external clock signals φ1 and φ2 and included "[i]nternal refresh circuitry [that] maintains data levels in the cells" (*i.e.*, was dynamic). (*See* 10311.) In addition, as stated above, the claims relate to a "synchronous semiconductor memory device" and it is clear that Bennett discloses that these types of memory devices were well known. (A1352-53(66:9-67:18); A10(¶B7).)

As the Board correctly determined and is presently undisputed, Bennett discloses a memory device comprising a User (*i.e.*, memory) implemented on the same chip substrate as the Versatile Bus Interface Logics and the memory device implements a synchronous communication protocol. (A5-6; A10.)

2. Synchronous Memory Devices and Interleaved Transactions

Rambus also discusses how synchronous memory devices permit interleaved transactions even though interleaving transactions are not recited anywhere in the claims. (Rambus's Br. 11-12.) To the extent such features are relevant, there is no dispute that Bennett discloses them. First, Rambus cannot dispute that Bennett discloses a synchronous memory device. (A1370(101:50-54) ("The timing diagram of FIG. 52a firstly shows as reference the signals (H)ϕ1 and (H)ϕ2 to which *all communication between the Versatile Bus Interface Logics and the User, and upon*

the Versatile Bus, is synchronously referenced") (emphasis added); A1339(40:52-55); A1337(35:59-62).)

Further, interleaved transactions are referred to in Bennett as pipelining where the bus may be used for other transactions during intervening cycles. (A1329(19:28-33).) In fact, the ability to perform interleaved transactions is one of the core objectives of Bennett. (A1329(19:28-33).) An example of Bennett's interleaved pipelined operations on a bus is shown in Figure 30, where the cycle between the beginning of transaction 1 and its completion is used to begin an additional transaction (*i.e.*, two outstanding requests). (A1362(85:5-6) (explaining that Figure 30 shows "three pipelined transactions"); *see also* A16 and A10021 (Respectively, the Board's and District Court's discussion of Bennett's memory transaction pipelining).)

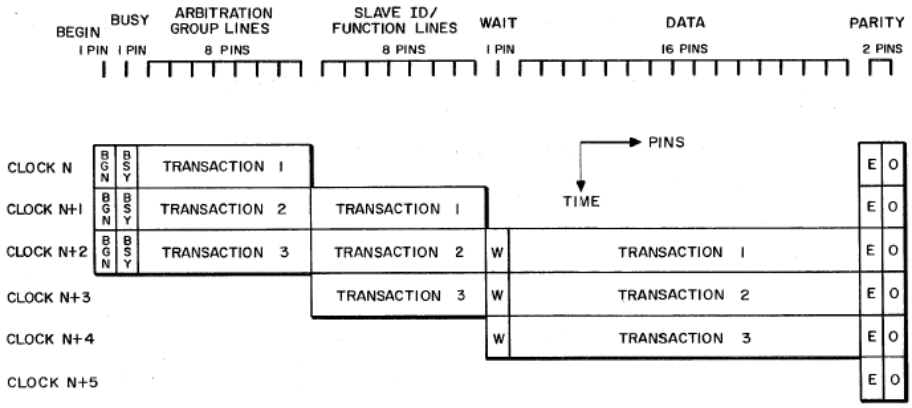


Fig. 30

Bennett FIG. 30 (A1084)

Thus, neither a synchronous memory device nor interleaved memory transactions were novel at the time the ’916 Patent was filed. In fact, both features are extensively disclosed by Bennett.

3. Memory Device Response Time in the ’916 Patent

Throughout its arguments, Rambus relies on the premise that the access times disclosed in the ’916 Patent specification are absolute in that read data is always output exactly when a certain number of clock cycles expires. (*E.g.*, Rambus’s Br. at 15, 17, 42.) However, the specification of the ’916 Patent repeatedly states that outputting data exactly at the expiration of the access time is merely a preferred implementation and not a necessary feature. For example, the ’916 Patent specification states:

> Thus an access time value of ‘1’ would indicate that the slave should not access the bus *until at least two cycles after* the last byte of the request packet has been received.

(A156(16:10-13) (emphasis added).)

> In a preferred implementation, semiconductor devices connected to the bus contain registers 172 which specify the memory addresses contained within that device and access-time registers 173 which store a set of one or more delay times at which the device can *or should* be available to send or receive data.

(A151(6:37-42) (emphasis added).)

> To reduce the complexity of the slaves [e.g., memory devices], a slave *should preferably respond* to a request in a specified time, sufficient to allow the slave to begin or possibly complete a device-internal

> phase including any internal actions that must precede the subsequent bus access phase.

(A152(8:54-58) (emphasis added).)

> *In most cases*, a slave will respond at the selected access time by reading or writing data from or to the bus over bus lines BusData[0:7] and AddrValid will be at logical 0.

(A154(12:1-3) (emphasis added).)

When viewed in light of the specification, it is clear that outputting data exactly when the access time transpires is only a preference and not a requirement. The specification shows that access time is at best a minimum time needed for the memory device to perform a transaction but that in other cases a memory device may not respond until some indeterminate number of clock cycles after the access time expires. (A156(16:1-13).)

Nor do claims 26 or 28 require that data be output exactly when a time period transpires because they recite only outputting data "after" an amount of time transpires. The claims certainly do not preclude an intervening arbitration time.[2] Even if arbitration occurs, the data is still output "after the amount of time transpires" which is all that claims 26 and 28 require.

[2] As Rambus points out (Rambus's Br. at 7), "arbitration" refers to a process by which a user, such as memory, competes with other users for access to the bus.

D. Summary of the Proceeding Prior to This Appeal

1. Anticipation Rejection Based on Bennett

On appeal to the Board, Micron argued that the examiner erred in withdrawing the anticipation rejection of Bennett. The examiner erroneously concluded that Bennett failed to disclose "a register which stores a value that is representative of an amount of time to transpire after which the memory device outputs the first amount of data" as recited in claim 26 of the '916 Patent. (A1611-16.) Micron noted that this was the only limitation in claim 26 that the examiner found absent in Bennett's disclosure.[3] (A1611.)

To illustrate the examiner's error, Micron pointed to the express disclosure in Bennett for Figures 25a and 25b. In Figure 25a, the configuration register stores the value 122121 as parameters I through VI. (A1612; A1362(85:49-86:41).) This configuration value results in a transaction cycle time of 4 clock cycles. (A1612; A1362(85:49-86:41).) In Figure 25b, the configuration register stores the value 122123 as parameters I through VI, which results in a transaction cycle time of 3 clock cycles. Thus, the change of parameter VI from 1 to 3 results in a "reduction in total transaction times from 4 clock cycles to 3 clock cycles." (A1362(86:31-41); A1612.) Likewise, the change of parameter VI from 3 to 1 inserts an

[3] In its respondent brief to the Board, Rambus also argued for other grounds to distinguish Bennett, but did not raise any of those grounds in its appeal to this Court. (A10427-A10432; A10437-A10438.)

additional clock cycle between the operation code and the output of data that results in a one clock cycle delay in outputting data. (A1612.)

Micron also argued that the examiner incorrectly determined that "the Wait Line does not 'represent' an amount of time" and erroneously concluded that "the configuration digit itself is not indicative of the number of 'clock cycles' that will have transpired before data is output." (A1614 (citing A1567).) Micron pointed out that a dedicated Wait Line within a configured memory results in the outputting of data one clock cycle earlier than an otherwise identical memory having a multiplexed Wait Line, as the examiner had agreed. (A1614 (citing A1567) (examiner acknowledging that "Figures 25a and 25b show[] that a change in the configuration value changes the number of clock cycles that transpire").)

Micron noted that the flaw in the examiner's decision that parameter VI does not represent the claimed delay time was that the examiner mistakenly compared two differently configured systems, Figures 35 and 36. (A1614.) The examiner found:

> As per figure 35, the configuration is 52252**3**55. In this example, the configuration wait digit is "3" which equates to 1 wait line. As shown in the figure the wait indication and the data occur in the same time cycle.
>
> As per figure 36, the configuration is 43153**3**55. In this example, the configuration wait digit is "3" (like Fig. 35) which equates to 1 wait line. As shown in the figure the data is output two cycles after the wait indication.

(A1567 (emphasis in original).)

The examiner, however, improperly compared two different configurations that included numerous changes to system parameters other the wait line parameter VI. (A1614.) Micron argued that the examiner's comparison of substantially different configurations does not rebut the fact that changing parameter VI from 3 to 1 when other parameter values remain constant would result in a one clock cycle delay in outputting data and that the precise time to transpire before data is output can be precisely determined. (A1614-1615 (illustrating this example with respect to the configuration of Figure 36.) In other words, the relevant inquiry is whether a change in parameter VI will change the time to transpire when the other configuration parameters are held constant.

Finally, even if Rambus were correct that other Bennett embodiments performed differently than Figures 25a and 25b, that would not be sufficient to overcome the anticipation rejection based on Figures 25a and 25b. *ArthroCare*, 406 F.3d at 1372 (only one embodiment needs to anticipate the claim).

2. Anticipation Rejections Based on JEDEC and Park

The '916 Patent purports to claim priority to the parent '898 application filed April 18, 1990. During reexamination, the examiner found that claims 26 and 28 of the '916 Patent were entitled to the priority date of the '898 application and refused

to adopt the anticipation rejections based on the intervening references, JEDEC and Park. (A10328-A10349.)

In its appeal to the Board, Micron argued that the examiner erred in determining that claims 26 and 28 are entitled to an effective filing date earlier than the February 27, 2001 filing date of the ’916 Patent. (A1617-1629.) Accordingly, the examiner erred in not adopting the rejections based on JEDEC and Park.

3. The Board’s Decision

Despite Micron’s showing that claims 26 and 28 lacked the required written description (because they do not claim the multiplexed bus interface of the invention described in the ’898 application), the Board disagreed with Micron and determined that the examiner did not err in determining that claims 26 and 28 of the ’916 Patent are entitled to the benefit of the April 18, 1990 filing date. (A23.1-A23.4.)

In the Decision issued June 14, 2012, the Board concluded that the examiner erred in withdrawing the anticipation rejection of claims 26 and 28 based on Bennett. (A51.) The Board made numerous factual findings to support the conclusion Bennett anticipates claims 26 and 28. First, the Board determined Bennett’s User Device is a single chip memory device. (A5-6(¶B1) (citing A1325(12:29-32) and A1337(35:59-61).) Second, the Board found that Bennett

discloses that those User memory devices are connected to a synchronous "Versatile Bus" and use the synchronous communications protocols disclosed in Bennett. (A6(¶B2, ¶B7.)

Third, the Board found that "Figures 25a-h represent generic slave devices and hence encompass memory devices." (A16.) As for the operation of Figures 25a-h, the Board found Bennett discloses that the precise number of clock cycles that transpire before outputting data is known and that the total number of clock cycles can be delayed one clock cycle by changing parameter value VI stored in the configuration register on the User Device:

> As Figures 25a-h show, relative to the ID/FUNCTION command, which includes a read or a write *(see e.g.* Fig. 35, 36), the sixth configuration digit 1 corresponds to an extra clock cycle, based on multiplexing, as compared to the total clock cycle number corresponding to the sixth configuration digit 3, based on pipelining. This extra clock cycle which occurs every time the sixth parameter digit is 1 in Figures 25a-h, amounts to four total clock cycles, or two clock cycles after a function command such as write (i.e., the ID/FUNCTION command). On the other hand, every time the sixth digit is 3 in Figures 25a-h, the delay amounts to three total clock cycles, or one clock cycle after the read or write command (i.e., ID/FUNCTION command). (*Compare* Figs. 25a, c, e, and g (sixth parameter 1) *with* Figures 25b, d, f, and h (sixth parameter 3); col. 85, 1. 9 to col. 87, 1. 6.).

(A8-9(¶B5) (footnote omitted).)

In its analysis, the Board found that Bennett's disclosure, depicted in Figure 25a and 25b, reads on the claim limitation of "a value that is representative of an

amount of time to transpire after which the memory device outputs the first amount of data." (A9; A13; A161(26:65-67).) In making this determination, the Board correctly construed the claim limitation in light of the '916 Patent's disclosure. (A13-14 (referring to A153(9:17-25).) The Board also determined that claim 26 does not specify when the representative time value starts to run and concluded that the claim limitation in dispute encompasses "any number of starting points 'after which' the 'representative' time 'value' starts and thereafter 'transpires.'" (A14.)

In particular, the Board found that Bennett begins transferring data transfer either (1) one clock cycle after receiving a read request, if the Wait signal and memory data are being transferred on different bus lines, or (2) two clock cycles after receiving a read request, if the Wait signal and memory data share the same bus line (*i.e.*, are multiplexed). (A14.) Whether or not the Wait and data bus lines are multiplexed depends on the sixth (VI) parameter value within the configuration register depicted in Figure 3 of Bennett. (A1068.) The Board found that a value of 1 in the sixth parameter signifies multiplexing the Wait signal with other data, resulting in transmission of data after an additional delay of one clock cycle. (A14.)

The Board further found that the sixth configuration parameter values presented a consistent pattern of delay. In particular, values of 3-5 for the sixth

parameter resulted in no delay, a value of 1 resulted in a delay of one clock cycle relative to the Wait signal, and the value of 2 likewise results in no delay since no Wait signal is employed. (A15.) The Board found that the evidence of record demonstrated that Bennett's system knows the specific timing relationship for each protocol configuration. (A16.) Moreover, the Board referenced the examiner's finding that changing the sixth parameter value from 3 to 1 as shown in Figures 25a and 25b results in an output delay of one clock cycle. The Board determined the examiner's finding was sufficient to satisfy claim 26's delay limitation. (A17.)

The Board also held that the examiner incorrectly compared the differently configured memories represented by Figures 35 and 36. The Board acknowledged the examiner's determination that Figures 35 and 36 each showed a different clock delay with respect to the wait signal for the same value of 3 for the sixth configuration parameter. (A17.) The Board reasoned, however, that this comparison was "incorrect" because it merely showed that "different embodiments" may result in different delays. (A17.) As the Board noted, the correct comparison of changing the sixth parameter value *within a single configuration* (*e.g.*, including Figure 36) shows that configuration satisfies the claim language. (A17-18). That is, the difference in total clock cycles of Figures 35 and 36 is due to differences in other configuration parameters. (A17.)

Next, the Board noted "[i]n oral argument, Rambus also raised a new argument" that Figure 35 of Bennett shows an indeterminate arbitration time. (A19.) Despite the fact this issue was not briefed by Rambus, the Board noted that this characterization was irrelevant because the memory device of Figure 35 could win arbitration on the first time and that Figure 35's arbitration depiction would not rebut the timing shown in other embodiments that do not rely on arbitration. The Board further determined, given claim 26 is not limited to specifying any particular signal to trigger the time delay, that the embodiment depicted in Figure 36 satisfies the limitation at issue when construed as "a value that is representative of any amount of time to transpire after which [a read acknowledgment signal from the memory device to the requestor] the memory device outputs the first amount of data." (A20.)

The Board also addressed Micron's appeal arguments that claims 26 and 28 were not entitled to the filing date of the '898 application and that JEDEC and Park were therefore prior art. In addressing Micron's arguments, the Board relied on *Rambus, Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1094-95 (Fed. Cir. 2003). There, in evaluating the district court's claim construction, the Court held that the "term 'bus' could not be read restrictively as a 'multiplexed bus' even though the patentee described the 'present invention' in terms of a 'multiplexed bus' in isolated portions of the specification because 'remainder of the

specification and the prosecution history shows that Rambus did not clearly disclaim or disavow such claim scope in this case.'" (A23.2 (quoting *Infineon*, at 1094-95).) The Board further addressed Micron's arguments by determining that "*Infineon's* claim construction analysis … implied that skilled artisans were in possession of generic bus claims." (A23.2.) The Board determined that the features of claim 26 could be practiced on both multiplexed and non-multiplexed buses in light of *Hynix Semiconductor, Inc. v. Rambus, Inc.*, 645 F.3d 1336, 1351-53 (Fed. Cir. 2011), which found that there was sufficient evidence to uphold the jury verdict of adequate written description for similar claims where the genus consisted of only two species, a multiplexed bus and a non-multiplexed bus. (A23.4.)

One of the matters about which Rambus requested reconsideration concerned the Board's interpretation of the term "representative" in the context of the claim. (*See e.g.*, A10457.) Just as it does in this appeal, Rambus argued that the proper frame of reference is measured from the receipt of the read operation code. (*Id*.) In the Board's Decision on Rehearing, the Board noted that Bennett was primarily analyzed from that exact frame of reference and thus Bennett anticipates under either Rambus's requested frame of reference or a broader frame of reference encompassed by the claims. (A40 (citing A14, A20).) The Board also noted how its findings on this issue are consistent with the findings made in

District Court. (A44 (citing *Rambus, Inc. v. Hynix Semiconductor, Inc*. 628 F.Supp.2d 1114, 1132-38 (N.D. Cal. 2008)).)

Finally, just as it does in its appeal to this Court, Rambus placed great emphasis on this Court's construction of "representative" for another patent in *Tehrani* v. *Hamilton Med. Inc.*, 331 F.3d 1355, 1361 (Fed. Cir. 2003). But the Board found Bennett's parameter values "represent," "dictate," "symbolize," or "stand for" a value of time, which is consistent with the meaning of representative in *Tehrani*. (A49.)

IV. SUMMARY OF THE ARGUMENT

Rambus argues that the Board erred in finding that Bennett anticipates claims 26 and 28 of the '916 Patent because (1) the Board allegedly misconstrued the term "representative" from the limitation "a value representative of an amount of time to transpire" recited in claim 26, (2) the Board erroneously held that the delay time can be measured starting with the "read acknowledgement signal" as opposed to immediately after the receipt of the request, and (3) the Board's factual findings lack substantial evidence (Rambus's Br. at 40, 45, and 48.)

Rambus, however, has failed to show that the Board erred in determining that claims 26 and 28 are anticipated by Bennett even under Rambus's construction of the term "representative." Figures 25a-h of Bennett disclose the claimed "value representative of an amount of time to transpire" (also referred to as the "delay

time") which is measured after receipt of the read request, because data is output after a delay of either one clock cycle or two clock cycles depending on the value set in the sixth parameter of the configuration register. (A14.)

Rambus also has failed to show that the Board erred when it found that the claims are anticipated by Bennett even under Rambus's incorrect claim interpretation. That is, even assuming that Bennett does not disclose outputting data a fixed period of time after receipt of a read request, which it does, Bennett still anticipates the claims of the '916 Patent because neither the claims nor the specification requires that the time to transpire be measured from the receipt of an operation code as opposed to another reference point.

The only error in the Board's decision was determining that claims 26 and 28 have priority to the April 18, 1990 filing date of the '898 application. (A23.1-23.4.)

V. ARGUMENT

A. Standard of Review

Rambus has the burden to show that the Board committed reversible error. *In re Watts*, 354 F.3d 1362, 1369 (Fed. Cir. 2004). Anticipation is a question of fact. *In re Baxter Travenol Labs*., 952 F.2d 388, 390 (Fed. Cir. 1991). What a reference teaches is a question of fact. *Para-Ordnance Mfg., Inc. v. SGS Imps. Int'l, Inc*., 73 F.3d 1085, 1088 (Fed. Cir. 1995).

This Court upholds the Board's factual findings unless those findings are not supported by substantial evidence. *In re Gartside*, 203 F.3d 1305, 1316 (Fed. Cir. 2000). Substantial evidence "is something less than the weight of the evidence but more than a mere scintilla of evidence," *In re Kotzab*, 217 F.3d 1365, 1369 (Fed. Cir. 2000), and "means such relevant evidence as a reasonable mind might accept as adequate to support a conclusion." *Consol. Edison Co. v. NLRB*, 305 U.S. 197, 229 (1938).

Further, if "the evidence in [the] record will support several reasonable but contradictory conclusions," then this Court "will not find the Board's decision unsupported by substantial evidence simply because the Board chose one conclusion over another plausible alternative." *In re Jolley*, 308 F.3d 1317, 1320 (Fed. Cir. 2002). "The possibility of drawing two inconsistent conclusions from the evidence does not prevent the Board's finding from being supported by substantial evidence." *Hoover Co. v. Royal Appliance Mfg. Co*., 238 F.3d 1357, 1361 (Fed. Cir. 2001).

Claim construction is a question of law that this Court reviews *de novo*. *In re NTP, Inc*., 654 F.3d 1268, 1274 (Fed. Cir. 2011) (citing *In re Baker Hughes, Inc*., 215 F.3d 1297, 1301 (Fed. Cir. 2000)). During reexamination proceedings, claims are given their broadest reasonable interpretation consistent with the specification.

In re Yamamoto, 740 F.2d 1569, 1571-72 (Fed. Cir. 1984); *Phillips v. AWH Corp*., 415 F.3d 1303, 1316 (Fed. Cir. 2005).

B. The Board Correctly Determined, Based on Substantial Evidence, That Bennett Discloses "A Value Representative of an Amount of Time to Transpire After Which the Memory Device Outputs the First Amount of Data"

1. The Board Correctly Determined That Bennett Anticipates Claims 26 and 28 Even Under Rambus's Construction of "Representative"

Rambus first argues that in order to be "representative," "a value must 'be directly related to and stand for, or be reasonable proxy for, the latter item.'" (Rambus's Br. at 41 (citing *Tehrani,* 331 F.3d at 1361.)[4] While Rambus couches this argument solely as a claim construction issue, it should be noted that the Board found that Bennett anticipates even using the construction of "representative" from *Tehrani*. The Board held "Bennett's parameters VI, VII, and VIII not only represent the delay time…, they *dictate* that time…in a direct manner." (A48 (emphasis in original).) [5] Moreover, the Board expressly held: "Bennett's configuration parameter values represent, 'symbolize,' or 'stand for,'…the delay

[4] As an initial matter, Rambus's reliance on *Tehrani* is misplaced, as *Tehrani* was decided under the now repudiated *Texas Digital* principals of claim construction. *Tehrani* 331 F.3d at 1361 (citing *Tex. Digital Sys., Inc. v. Telegenix, Inc*. 308 F.3d 1193, 1203 (Fed. Cir. 2002)). The meaning that "representative" had in *Tehrani* is of little, if any, value in determining how the term should now be construed for the '916 patent.

[5] Parameters VII and VIII are directed towards the limitation relating to "block size information," which is not currently at issue in Rambus's appeal to this Court.

time…since they dictate that time." (A48-49 (citing *Tehrani*, 331 F.3d at 1361).) Thus, the finding that Bennett anticipates under the construction argued for by Rambus should be reviewed for substantial evidence.

To the extent the Board relied on a broader construction of "representative," such construction was based on the usage of "representative" in the '916 Patent. (A49; *compare Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*)("During patent examination, the pending claims must be 'given their broadest reasonable interpretation *consistent with the specification*.'")(emphasis added).) As the Board determined, the '916 Patent relies on encoding schemes so that the same value stored in a register "represents" multiple different numbers of clock cycles depending on which encoding scheme is selected. (A49.) As an example, the '916 Patent discloses the 3-bit pattern of 011 can "represent[]" either a value of 3 or 64 depending on what encoding scheme is selected by a separate parameter. (A154(11:44-64).)

Thus, in the '916 Patent, the number represented by a 3-bit pattern can change depending on the value of other configuration parameters. This is no different than Bennett, where the time to transpire represented by the 3-bits of configuration parameter VI may change depending on the value of other configuration parameters.

Even Rambus concedes that the actual time to transpire need not be stored in a register so long as a value representing that time is stored. (Rambus's Br. at 42 ("the access-time register stores *actual* predetermined delay times (or values representing them), corresponding to the *actual* 'timing of the response.'") (emphasis in original) (referencing A153(9:65-66).) Ramus's implicit argument is that masters in Bennett do not know the actual response timing of the slave memory devices. That argument contradicts the explicit disclosure in Bennett and the Board's factual findings that Bennett's communication protocol defines when data is transmitted. (A16 (quoting A1339(39:31-34).) Even without such disclosure, Rambus's argument is legally improper because it presumes that Bennett is inoperable as Bennett's interconnect system could not operate without knowledge of the timing of transactions, including memory transactions. *In re Sasse*, 629 F.2d 675, 681-82 (CCPA 1980) (prior art is presumed enabled and operable).

Rambus also attempts to show that the Board misconstrued "representative" by mischaracterizing the Board's use of the term "capability." Rambus argues that the Board construed "representative" to mean the "'capability' to represent [the] amount of time" to transpire, but only at certain times such as when the memory wins arbitration on the first attempt. (Rambus's Br. at 43.) In making that argument, Rambus relies on the following statement in the Board's decision: "This

characterization ignores the fact that the memory device can win arbitration on the first instance. Claim 26, a device claim, only requires this *capability*." (A19 (emphasis added).)

Rambus misinterprets the point of the Board's statement. The Board's use of the term "capability" was not for purposes of construing "representative" but rather for clarifying that claim 26 is broad enough to encompass a prior art memory device that discloses the capability of winning arbitration on the first attempt. The Board clarified this statement in its Decision on Rambus's Request for Rehearing stating:

> Rambus argues that Figure 35 reveals "an indeterminate amount of time before data is output by the memory" even if the device does win arbitration the first time. (Reh'g Req. 9.) But even if Figure 35 is relevant to the inquiry, it shows, after winning arbitration, the same data to function delay as other memory devices using a 3 for Parameter VI (e.g., Figures 25b). (*See* Bennett, col. 95, 11. 18-27; Bd. Dec. 17-18.) Rambus's other argument that not winning arbitration shows a lack of a correlation is not commensurate in scope with *the claims which do not require arbitration*.

(A44 fn.8 (emphasis added).) Thus, the Board's use of the term "capability" was in reference to anticipatory disclosure of the prior art and not with reference to the construction of the term "representative."

As demonstrated above, Rambus has not shown that the Board erred in determining that Bennett anticipates "a value that is representative of an amount of time to transpire" as recited in claim 26 of the '916 Patent. In relying on the

configurations shown in Figures 25a and 25b of Bennett, and more particularly on embodiments that do not require arbitration, the Board correctly determined that Bennett anticipates the claims, both under Rambus's construction of the term "representative" and under the proper construction of "representative" as derived from the '916 patent.

2. The Board Correctly Determined that the Claims Do Not Require the Delay Time to be Measured "Immediately After" Receipt of the Read Request

In response to the Board's alternative grounds for rejecting the claims based on a broad scope due to a lack of a timing reference point,[6] Rambus argues that the Board erred in determining that "'claim 26 does not specify any particular signal to trigger the time delay.'" (Rambus's Br. at 45-46 (citing A20.) Specifically, Rambus argues that the Board erred in finding that "the delay time in claim 26 can be measured starting with a 'read acknowledgment signal' (i.e., a follow-up signal sent from the memory back to the requester), as opposed to measuring the delay time from the receipt of the read request." (Rambus's Br. at 45-46 (emphasis omitted) (referencing A20).)

[6] The Board noted that "Despite this lack of a recited starting frame of references in claims 26 and 28, the Decision primarily explains how Bennett satisfies the claims based on a frame of reference" argued for by Rambus. (A40) Thus the decision determined that Bennett anticipates under either Rambus's narrow interpretation or the Board's broader interpretation of claims 26 and 28.

Rambus relies principally on the claim limitation reciting "output the amount of data in response to the first operation code and after the amount of time transpires." (Rambus's Br. at 46 (citing A162(27:1-3).) Yet, the phrase "in response to the first operation code" is directed to the "amount of data" and not to the "amount of time transpires." This is made clear by the usage of the same language in the limitation reciting "wherein the block size information is representative of *an amount of data to be output* by the memory device *in response to a first operation code*." (A161(26:62-64)(emphasis added).) Thus, the proper reading of the claim is that the amount of data to be transferred is responsive to the block size information received in the operation code. There is nothing in the claim indicating that the amount of time to transpire is even received from the operation code, let alone starts counting "in response to the first operation code."

Even if the amount of time to transpire were "in response to the first operation code" as Rambus suggests, that language still does not mean that the time to transpire must start running immediately after reception of the operation code. At most, it is the amount of time to transpire that is determined in response to the operation code and not when the time to transpire begins.

Notwithstanding the above, even if the time to transpire "begins immediately after receipt of a transaction request" as Rambus argues, the Board still correctly determined that Bennett anticipates. The Board expressly held: "Despite this lack

of a recited starting frame of reference in claims 26 and 28, *the Decision primarily explains how Bennett satisfies the claims based on a frame of reference defined by 'receipt of an operation code.'*" (A40 (emphasis added).)

Specifically, the Board made the following factual finding:

> Figures 25a-h show, *relative to the ID/FUNCTION command, which includes a read or write*…the sixth configuration digit 1 corresponds to an extra clock cycle, based on multiplexing, as compared to the total clock cycle number corresponding to the sixth configuration digit 3, based on pipelining. This extra clock cycle which occurs every time the sixth parameter digit is 1 in Figures 25a-h, amounts to four total clock cycles, or *two clock cycles after a function command such as a write (i.e., the ID/FUNCTION command)*. On the other hand, every time the sixth digit is 3 in Figures 25a-h, the delay amounts to three total clock cycles, or *one clock cycle after the read or write command (i.e., ID/FUNCTION command)*.

(A9(¶B5) (emphasis added).)

Based on this finding, the Board determined that "[data] transfers occur either one clock cycle or two clock cycles after the initial ID/FUNCTION (write or read) command in Figures 25a-h." (A14.) Accordingly, even based on the reference point asserted by Rambus (*i.e.*, after receipt of the read request), the Board correctly determined that Bennett anticipates because Bennett discloses that data is output either one clock cycle or two clock cycles *after the read request* in Figures 25a-h. (A14.)

3. The Board's Findings Are Supported by Substantial Evidence

Rambus argues that "[t]he Board did not rebut the examiner's finding that the same wait-line setting of 3 in configuration value VI of Bennett 'causes

different delays' in the transactions illustrated in Figures 25*b*, 35, and 36." (Rambus's Br. at 49 (citing A15).) Rambus's argument is flawed on several grounds. First, the Board is not required to "rebut the examiner's findings" as Rambus demands. "[T]he Board's primary role is to review adverse decisions of examiners including the findings and conclusions made by the examiner." *Ex parte Frye*, 94 USPQ2d 1072, 1077 (BPAI 2010) (precedential); *see also* 35 U.S.C. § 6(b) (2002).[7] "Specifically, the Board reviews the particular finding(s) contested by an appellant anew in light of all the evidence and argument on that issue." *Frye*, 94 USPQ2d at 1075. The Board does, of course, "necessarily weigh all of the evidence and argument" when it is reviewing findings of the examiner anew. *Id*. (quoting *In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992)).

Under the PTO's review procedures, no deference should be given to the examiner with respect to determinations of fact or law. The former PTO director has explained the PTO's review procedures in light of the decision in *Frye*:[8] "This means that the Board does not give deference to positions taken by the examiner when considering an appellant's argument specifically challenging the examiner's findings." http://www.uspto.gov/blog/director/entry/ex_parte_frye_bpai_s. The Director's reasoning is supported by this Court's case law as well. *See In re Berg*,

[7] The current version of § 6(b) (P.L. 112-283, Sept. 16, 2012, approved 1-15-13) enumerates the Board's duties.

[8] *Ex parte Frye* was decided in part by former Director Kappos.

320 F.3d 1310, 1315 (Fed. Cir. 2003) ("examiners *and administrative patent judges on the Board* are responsible for making findings…as to the meaning of prior art references to persons of ordinary skill in the art and the motivation those references would provide to such persons") (emphasis added).

Indeed, in reversing the examiner's determination, 37 C.F.R. § 41.77(a) requires only that the Board provide an opinion in support of its decision, but does not require the Board to detail the error in the examiner's findings. Therefore, neither the statute nor the rule requires the Board to explain error in the examiner's underlying findings in order to draw a different conclusion. Moreover, 37 C.F.R. § 41.77(b) provides that the Board may issue a new ground of rejection "should the Board have knowledge of any grounds not raised in the appeal for rejecting any pending claim…." Therefore, the Board can issue a new rejection based on its own factual findings even without reliance on factual findings of an examiner.

Here, the Board reviewed the parties' arguments and the examiner's position for withdrawing the grounds of rejection. As discussed herein, the Board found error in the examiner's position and, contrary to Rambus's argument, provided the reason for finding error. (*See, e.g.,* A17.) The Board provided its relevant findings of fact, legal authority, and analysis necessary to address the issue of whether claims 26 and 28 are anticipated in light of the prior art.

Next, even assuming the examiner's findings should be accorded some amount of deference, which they should not, the examiner nevertheless incorrectly found that the same wait-line setting of 3 in parameter VI causes different delays in the transactions illustrated in Figures 25b, 35, and 36. Rambus argues that "in the three transactions illustrated in Figures 25b, 35, and 36, there are three different transaction times, despite configuration parameter VI being set to '3' in each case." (Rambus's Br. at 50.) However, Rambus ignores that if configuration parameter VI of either Figures 25b or 36 were changed from 3 to 1, then the data would be provided *one clock cycle later*. (A19.) Thus, there can be no dispute that a setting of 1 in parameter VI for Figures 25b and 36 represents *one extra clock cycle delay*.

The exact change in the number of clock cycles to transpire when parameter VI is changed from 3 to 1 in both Figures 25b and 36 is easily determined and definitively known by Bennett's communication protocol. Regarding Figure 25b, using configuration 122123XX, the number of clock cycles between receipt of the operation code and transfer of data is one. (A1079.) If parameter VI in Figure 25b is changed from 3 to 1, and all other configuration parameters are held constant, the number of clock cycles increases to two. (A1079.) Similarly, regarding Figure 36, using configuration 43153355, the number of clock cycles between receipt of the operation code and transfer of data is one. (A1089). If parameter VI is changed to 1, and all other configuration parameters are held constant, the number of clock

cycles increases to two. This is because multiplexing the Wait signal (abbreviated WT in Figure 36) would tie up the bus for an additional clock cycle before transmission on the data pins could begin. That these embodiments read on the claim is sufficient to show anticipation, even if other embodiments do not. *ArthroCare*, 406 F.3d at 1372 (only one embodiment needs to anticipate the claim).

Figure 35 depicts a split transaction bus where the memory device potentially loses arbitration (A1366(94:57-60)), and Rambus's argument here is that the memory device must always respond at the programmed time, *i.e.*, that the possibility of an additional un-programmed delay defeats anticipation. This argument fails for at least two reasons. First, the claim language does not include the "always" limitation Rambus seeks. Indeed, the '916 Patent is replete with examples showing that responding exactly at a selected time is merely preferred rather than necessary and that a memory device may not always be able to respond exactly at the programmed time. (A154(12:8-12); A151(6:37-42); A152(8:54-58); A154(12:1-12); A156(16:10-13).)

Second, Bennett discloses embodiments that are not subject to arbitration, and therefore, always respond at the configured time. For example, Bennett discloses the slower speed of Large Memory "warrants freeing the interconnect for other transactions" (i.e., requires the Large memory to arbitrate to re-gain bus

access) while Fast Memory would not lose bus access requiring arbitration to re-gain bus access. (A1366(94:28-32).) In addition, even for embodiments subject to arbitration the memory device can win arbitration in the first try in which case the exact number of clock cycles to transpire is easily calculated just as with Figures 25b and 36, shown above.

In an attempt to rebut the fact that Figures 25a and 25b alone anticipate the claim, Rambus baldly asserts that Figures 25a and 25b are presented "in a hypothetical, generic manner in order to 'simplify' their presentation." (Rambus's Br. at 51.) Yet, nowhere does Bennett describe these transactions as hypothetical. Just as with the other figures, Figures 25a and 25b are provided as examples to help one understand the disclosure of Bennett. That Bennett would provide simple examples first only makes logical sense before providing the more complex examples found later in Bennett's disclosure. Bennett even tells the reader to "reference FIGS. 25a-25h" in understanding the effect of the configuration parameters on transaction timing. (A1328(17:32-29).)

Rambus has provided no case law or rationale why a simple example shown in the prior art cannot be used as an anticipatory disclosure. There is nothing in Bennett indicating that the examples shown in Figures 25a and 25b would not operate within Bennett. Bennett discloses just the opposite, as the configuration values given for Figures 25a and 25b are all within the "preferred embodiment" of

the configuration values shown in Figure 3. (A1338.) Even Rambus admits that "[e]ach of these configurations…is within the preferred 'envelope' outlined in Figure 3 and is fully compatible with that preferred configuration." (Rambus's Br. at 49.)

Despite acknowledging that Figures 25a and 25b disclose an additional one clock cycle delay (Rambus's Br. at 40), Rambus argues that parameter VI cannot be "representative" of an amount to transpire because it merely specifies the number of wait lines and has "nothing to do with the concept of predetermined delay times." (Rambus's Br. at 21-23, 41.) However, the purpose of the Wait signal is not relevant for anticipation. *Toshiba Corp. v. Imation Corp.*, 681 F.3d 1358, 1367-68 (Fed. Cir. 2012) (overturning a claim construction that improperly read a purpose requirement into a limitation reciting "identifying information represents the number of recording planes"). Just as in *Toshiba*, the claims here recite structural elements and, therefore, the purpose of Bennett's configuration parameter VI is irrelevant since configuration parameter VI discloses the structural elements of claims 26 and 28.

Rambus continues: "[i]n the real world, however, these 'simplified' assumptions are not always true," because arbitration and other variables must be considered. (Rambus's Br. at 52-53.) However, sometimes the "simplified" assumptions are true, for example, in systems that do not require arbitration.

(A1366(94:28-32).) Moreover, as the Board noted, "Rambus does not dispute this underlying rationale or the specific finding that in Figures 25a-h, the number 1 always results in a two clock cycle delay for DATA after a write request, and the programmable number 3 always results in a one clock delay for DATA after a write request." (A41-42.) Thus, at a minimum, Figures 25a and 25b provide the "predictability" and "consistency" that Rambus argues is required of claims 26 and 28.

Rambus's allegation that Figures 25a and 25b do not relate to memory transactions has been thoroughly reviewed and dismissed by both the Board and District Court, both of which found that Figures 25a and 25b represent transactions of a "memory device." (A16 (holding "Figures 25a-h represent generic slave devices and hence encompass memory devices"); A10022 (District Court referring to Figures 25a and 25b as representing a "memory device").)

Rambus reiterates its arguments that the Board's claim construction is erroneous. Micron has already addressed why the Board's claim construction was proper above. However, even if this Court agrees with Rambus's claim construction, there is still no dispute that Figures 25a and 25b would anticipate the claim based on the findings by the Board.

Finally, the premise of Rambus's argument – that the same outcome must occur in every single one of Bennett's 30,000+ configurations in order to show

anticipation – results in the fundamentally flawed conclusion that Bennett's vast disclosure would provide virtually no anticipatory disclosure due to its high configurability. Instead, as the Board has determined, at least some embodiments in Bennett's highly configurable system anticipate the claim, which is all that is legally required even if certain other configurations would not anticipate. *ArthroCare*, 406 F.3d at 1372.

C. Alternatively, the Board Erred in Not Adopting the Anticipation Rejections Based on JEDEC and Park

Alternatively, in addition to the Bennett rejection discussed above, JEDEC and Park anticipate claims 26 and 28 of the '916 Patent. The Board and the examiner erred in determining that claims 26 and 28 are entitled to the earlier filing date of the '898 application, which was the only basis for not adopting Micron's proposed rejections based on JEDEC and Park. As Micron argued on appeal to the Board, claims 26 and 28 are not entitled to an earlier filing date because claims 26 and 28 are so different from the "invention" described in the specification of the original '898 application that the right of priority to those earlier applications was lost. (A1617-1629.)

Claims 26 and 28 are not limited to the type of "bus" over which the memory device communicates with the rest of the system. The '898 parent application, to which the '916 Patent purports to claim priority, is explicit that the bus must be a "multiplexed" bus, where the various address, data, and control

information is carried over the same plurality of bus lines, and is "multiplexed" so that the different information is carried at different times. Accordingly, Micron showed that because claims 26 and 28 broadly encompasses any "bus" that would connect the memory to the rest of the system, those claims have no written description support in—and no priority to—the '898 parent application, which describes only a "multiplexed" bus for reading or writing data.

In rejecting Micron's arguments, the Board based its decision on its belief that the priority determination was controlled by the claim construction adopted by this Court in *Infineon*, 318 F.3d at 1094-95. (A23.1-23.4.) That belief is incorrect. In a post-*Infineon* case involving priority issues as raised in this appeal, this Court stated: "*Though it would certainly be reasonable to conclude that Rambus's claims do not meet the written description requirement on the basis of ICU Med*., that argument was presented to the jury and rejected by it." *Hynix Semiconductor Inc. v. Rambus Inc.*, 645 F.3d 1336, 1352-1353 (Fed. Cir. 2011) (referring to *ICU Medical, Inc. v. Alaris Medical Systems, Inc.*, 558 F.3d 1368 (Fed. Cir. 2009) (emphasis added)).

The Court's statements in *Hynix* show that the *Infineon* claim construction ruling is not dispositive of the written description priority issue. As in *Hynix*, and as further detailed below, "it would certainly be reasonable to conclude that Rambus's claims do not meet the written description requirement on the basis of

ICU Med." *Hynix*, 645 F.3d at 1352-53. Moreover, unlike in *Hynix*, there is no jury verdict that constrains this Court's determination of the priority issue.

As shown below, the evidence demonstrates that claims 26 and 28 of the '916 Patent are not entitled to the filing date of the '898 application. Thus, JEDEC and Park are prior art and should have been applied by the Board to reject claims 26 and 28.

1. The Board Relies on an Improper Legal Standard for Priority Written Description

The Board upheld the examiner's determination of priority based on this Court's decision in *Infineon* that the claim construction of "bus" was not limited to a multiplexed bus. (A23.1-23.4.) Although Micron argued that *Infineon* did not apply to the section 112/120 issue in this proceeding, the Board improperly concluded:

> Micron's contentions are unconvincing to show that *Infineon* was wrongly decided or would somehow require reaching a different result based on a written description priority analysis as opposed to its claim construction analysis.

(A23.1-23.2 (incorporating by reference related PTAB decisions).)

Nevertheless, the Board is incorrect that an analysis of written description priority would have the same result as this Court's claim construction analysis in *Infineon*. This Court recognizes that a patentee may prevail on a broad claim construction, only to have the patent later declared invalid for failure to include a

written description of sufficient breadth. *See, e.g., Ariad Pharms., Inc. v. Eli Lilly & Co.*, 560 F.3d 1366, 1377 (Fed. Cir. 2009).

Notably, in deciding *Hynix*, this Court cited *Infineon* only with respect to claim construction and not regarding written description. *Hynix*, 645 F.3d at 1349-53. Thus, even if *Infineon's* claim construction is correct that "bus" is not limited to a "multiplexed bus," that fact alone does not mean the specification of the '898 application provides written description support for a non-multiplexed bus as determined by the Board.

2. Proper Legal Standard for Determining Priority Written Description

In order for a patent claim to receive the benefit of an earlier filing date under 35 U.S.C. § 120, the invention as claimed must have been "disclosed in the manner provided by the first paragraph of section 112 of this title [in the earlier application]." 35 U.S.C. § 120; *see also Tronzo v. Biomet, Inc.*, 156 F.3d 1154, 1158 (Fed. Cir. 1998). The first paragraph of section 112 requires "a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention." 35 U.S.C. § 112, ¶ 1.

Courts have found three requirements encompassed by this language: "[1] describe, [2] enable, and [3] set forth the best mode." *Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co*., 535 U.S. 722, 736 (2002); *Ariad*, 598 F.3d at 1343. The issue here is whether the "invention" recited in claims 26 and 28 was described in the manner required by § 112 in the original '898 application in order to establish priority under § 120.

The written description requirement's purpose is to "ensure that the scope of the right to exclude, as set forth in the claims, does not *overreach the scope of the inventor's contribution* to the field of art *as described in the patent specification.*" *Univ. of Rochester v. G. D. Searle & Co., Inc.*, 358 F.3d 916, 920 (Fed. Cir. 2004)(emphasis added). This Court recently reaffirmed this important statutory requirement *en banc* in *Ariad*, explaining that "the description must 'clearly allow persons of ordinary skill in the art to recognize *that [the inventor] invented what is claimed*.'" *Ariad*, 598 F.3d at 1351 (emphasis added); *see also id.* ("[T]he test for sufficiency is whether the disclosure of the application relied upon reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date").

Two recent decisions from this Court have provided guidance regarding the written description requirement. In *LizardTech, Inc. v. Earth Resource Mapping, Inc.*, 424 F.3d 1336 (Fed. Cir. 2005), the Court was faced with two similar

independent claims (claims 1 and 21). *Id.* at 1340. Claims 1 and 21 were both directed to image processing on a computer using a discrete wavelet transformation (DWT) based compression process. *Id.* at 1340. Nevertheless, while claim 1 recited the specific way to calculate the DWT that was described in the specification, claim 21 recited the process generically. The Court affirmed the invalidity of claim 21 based on a written description violation because claim 21 was broader than the specification could support:

> The fact that claim 21 is directed to creating a seamless DWT does not mean that the claim is valid, however. The problem is that the specification provides only one method for creating a seamless DWT, which is to "maintain updated sums" of DWT coefficients. That is the procedure recited by claim 1. Yet claim 21 is broader than claim 1 because it lacks the "maintain updated sums" limitation. Thus, a person of ordinary skill in the art would understand that claim 21 is directed to a seamless DWT. But because there are no limitations in claim 21 as to how the seamless DWT is accomplished, claim 21 refers to taking a seamless DWT generically.

Id. at 1344.

A key factor discussed by the Court in finding claim 21 invalid was that the broad generic claim 21 covered "prior art that suffers from precisely the same problems that the specification focuses on solving." *Id.* at 1343-44. In other words, by describing how the disclosed invention differs from the prior art, a specification defines both what the disclosed invention is, and importantly, what it is not.

The *LizardTech* decision also provided the following informative analogy:

> [S]uppose that an inventor created a particular fuel-efficient automobile engine and described the engine in such detail in the specification that a person of ordinary skill in the art would be able to build the engine. Although the specification would meet the requirements of section 112 with respect to a claim directed to that particular engine, it would not necessarily support a broad claim to every possible type of fuel-efficient engine, no matter how different in structure or operation from the inventor's engine.

Id. at 1346.

More recently, in *ICU Medical, Inc.*, this Court addressed a claim that failed to recite an element of the invention described in the specification. The patent at issue in *ICU Medical* was directed to a medical valve. *ICU Medical*, 558 F.3d at 1377. All valves described in the patent specification included a "spike"; however, the relevant claims did not require a spike. *Id.* The Court referred to the "claims as spikeless not because they exclude the preferred embodiment of a valve with a spike but rather because these claims *do not include a spike limitation*." *Id.*(emphasis added). The patentee argued that the claims were "neutral regarding whether the valve must include a spike," and therefore, covered either the presence or absence of a spike. *Id.* The Court found that the patentee violated the written description requirement by attempting to broaden the claims to exclude an element of the disclosed invention:

> [The] asserted spikeless claims *are broader than its asserted spike claims because they do not include a spike limitation*; these spikeless claims thus refer to medical valves *generically*—covering those

> valves that operate with a spike ***and*** those that operate without a spike. But the specification describes only medical valves with spikes.

Id. at 1378 (emphasis added).

3. The Memory Device "Invention" Disclosed in the '916 Patent Requires an Interface to a Narrow Multiplexed Bus

In resolving the issue of whether claims 26 and 26 of the '916 Patent are entitled to claim priority to the '898 application, the first step is to determine what "invention" is described in the '898 application. *Tronzo*, 156 F.3d at 1159 (explaining that the asserted patent "describes the *invention* as a 'trapezoid,' a 'truncated cone,' or a cup of 'conical shape'")(emphasis in italics added).

As the following analysis shows, the "invention" of the '898 application required a bus interface that includes signal lines over which substantially all address, data, and control information is carried. Because the address, data, and control information is carried over the same lines, the information must be "multiplexed," or "time shared," in that each of the different types of information (address/data/control) is sent over the common set of bus lines at different times. (*See* A10538(42:20); see also A10625(Fig.6).) The '898 application describes in detail this "multiplexed bus" invention.

From its very start, the '898 application makes clear that the "invention" is directed to a new "bus" interface and architecture. The "Field of the Invention" describes the "invention" as follows:

> An integrated circuit *bus interface* for computer and video systems is described which allows high speed transfer of blocks of data, particularly to and from memory devices, with reduced power consumption and increased system reliability. A new method of physically implementing *the bus architecture* is also described.

(A10497(1:10-15)(emphasis added).) The "new bus interface" is also described as "[o]ne *object of the present invention*." (A10502(6:8-9)(emphasis added).) Another "object of the invention" is described as "a method for transferring address, data and control information over a relatively narrow bus." *(*A10502(6:22-23).)

Similarly, the "Summary of the Invention" explains that the "present invention" requires memory devices to be connected to this disclosed narrow multiplexed bus:

> The *present invention* includes a memory subsystem comprising at least two semiconductor devices, including at least one memory device, *connected in parallel to a bus, where the bus includes a plurality of bus lines for carrying substantially all address, data and control information needed by said memory devices*, where the control information includes device-select information and *the bus has substantially fewer bus lines than the number of bits in a single address, and the bus carries device-select information without the need for separate device select lines connected directly to individual devices*.

(A10503(7:10-19)(emphasis added).) Indeed, the very next paragraph describes how the prior art must be "modified" in accordance with the purported invention to allow such memory devices to include an interface to the "new bus":

> [A] standard DRAM 13, 14, ROM (or SRAM) 12, microprocessor CPU 11, I/O device, disk controller or other special purpose device such as a high speed switch is modified to use a wholly bus-based

> interface rather than the prior art combination of point-to-point and bus-based wiring used with conventional versions of these devices. *The new bus* includes clock signals, power and *multiplexed address, data and control signals*.

(A10503(7:20)-A10504(8:2)(emphasis added); *see also* A10504(8:25)-A10505(9:3) ("New bus interface circuits *must be added* and the internals of prior art DRAM devices *need to be modified* so they can provide and accept data to and from the bus at the peak data rate of the bus") (emphasis added).)

The '898 application also explains how the multiplexed bus interface is used within the disclosed system:

> *In the system of this invention*, DRAMs and other devices *receive address and control information over the bus and transmit or receive requested data over the same bus*. Each memory device contains only a single bus interface with no other signal pins.

(A10504(8:9-13)(emphasis added).) Thus, the new bus interface uses the same bus lines to carry address, control, *and* data information. Moreover, the patent excludes the possibility of signal pins (connections to signal lines) other than to the address/control/data bus lines.

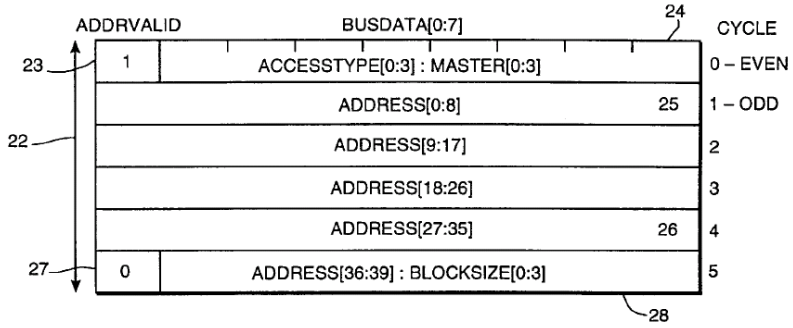
The Detailed Description also consistently describes the "present invention" as requiring devices adapted to interface to this narrow multiplexed bus:

> The *present invention is designed to provide a high speed, multiplexed bus* for communication between processing devices and memory devices *and to provide devices adapted for use in the bus system*. . . . The bus consists of a relatively small number of lines connected in parallel to each device on the bus. *The bus carries substantially all*

> *address, data and control information needed by devices for communication with other devices on the bus*.

(A10507(11:16-25)(emphasis added).)

The fact that each bus line carries multiple types of information is also shown in Figure 4 (reproduced below).



’898 application at FIG. 4

Although the ’898 application describes certain embodiments of the multiplexed bus interface as “preferred” or “examples,” (*see, e.g.*, A10505(9:16-18)(providing specific stub capacitances and inductances); A10508(12:8-10)(using 40-bit addresses)), the ’898 application never describes the narrow multiplexed bus interface itself as merely preferred or exemplary. Nor does the ’898 application describe any alternative bus interface structure. Instead, the clear and unambiguous disclosure is that the “new bus” interface is a necessary part of the purported invention

The original claims of the ’898 application directed to sending or receiving data are limited to devices adapted to interface to the narrow multiplexed bus by reciting a “bus including a plurality of bus lines for carrying substantially all

address, data and control information needed by said memory device." (*See*, *e.g.*, A10559(63:4-6)(claim 1); *see also id.* at independent claims 13, 25, 46, 56, 68, 82, 95, 97, 103, 106, 108, 111, 114, 116, 118, 121, 124, and 135 at A10561; A10565; A10572; A10577; A10582; A10589; A10596-A10597; A10599-A10608; A10613-10614.)

Indeed, only two original independent claims did not expressly describe interfacing to the multiplexed bus: claim 73, which is directed to the specific early/late clocking scheme disclosed in the '898 application, and claim 91, which is directed to the specific packaging scheme disclosed in the '898 application. Neither of those claims is directed to sending or receiving data to or from a memory device. The '898 application separately described the specific early/late clock and specific packaging scheme described in the specification as separate inventions. (*See* A10501(5:19-20)("The clocking scheme used in this invention has not been used before"); A10502(6:13-15)("Another object of this invention is to provide a clocking scheme to permit high speed clock signals to be sent along the bus with minimal clock skew between devices."); A10538(42:7)("Low Power 3-D Packaging"); A10538(42:19)("an innovative 3-D packaging technology").)

4. The "Prior Art" to the '898 Application Was Distinguished Based on the Bus and Interface Structure

In addition to the above passages describing the "invention" disclosed in the '898 application, a second important source of information comprises the '898

application's description of what the invention is not. *LizardTech*, 424 F.3d 1343-44.

In the Background of the Invention, the applicants distinguished the prior art from the claimed invention as separating the address lines, data lines, and control lines:

> Each memory device typically is connected in parallel to a series of *address lines* and connected to one of a series of *data lines*. When the computer seeks to read from or write to a specific memory location, an address is put on the address lines and some or all of the memory devices are activated using a separate *device select line* for each needed device.

(A10497(1:22-28)(emphasis added.)

The '898 application also includes a "Comparison With Prior Art" section, in which purported differences between the disclosed "invention" and the prior art are discussed. All but one reference is distinguished on the basis that it does not disclose the multiplexed bus.

- In distinguishing U.S. Patent No. 3,821,715 to Hoff *et al.*, the application states, "*most important, not all of the interface signals between the devices are bused* (the ROM and RAM control lines and the RAM select lines are point-to-point)." (A10499(3:15-18)(emphasis added).)
- In distinguishing U.S. Patent No. 4,315,308 to Jackson, the application states, "again, *not all of the interface signals are bused*." (A10500(4:2-3)(emphasis added).)
- In distinguishing U.S. Patent No. 4,449,207 to Kung *et al.*, the application states, "[t]he external interface to this DRAM is *conventional, with separate control, address and data connections*." (A10500(4:6-7)(emphasis added).)

- In distinguishing U.S. Patent Nos. 4,764,846 and 4,706,166 to Go, the application states, "[the disclosed] pages are difficult to use *because of point-to-point* wiring required to interconnect conventional memory devices with process elements . . . . No attempt is made to solve the problem *by changing the interface*." (A10500(4:10-14)(emphasis added).)

- In distinguishing U.S. Patent No. 3,969,706 to Poebsting *et al.*, the application states, "[t]he address is two-way multiplexed, *and there are separate pins for data and control* (RAS, CAS, WE, CS). The number of pins grows with the size of the DRAM, and many of the connections must be made point-to-point in a memory system using such DRAMS." (A10500(4:16-20)(emphasis added).)

- In distinguishing "backplane buses" in general, the application states "[n]one of the buses described in patents or other literature use only bused connections. All contain some point-to-point connections on the backplane." (A10501(5:13-15).)

- Finally, in distinguishing U.S. Patent No. 4,646,279 to Voss, the application states "[t]he rest of the interfaces to the DRAM (RAS, CAS, multiplexed address, etc.) remain the same as for conventional DRAMs." (A10502(6:5-7).)

The only prior art reference described in the "Comparison With Prior Art" section for which a bus structure was not discussed is U.S. Patent No. 4,247,817 to Heller, in which the clocking scheme, rather than the transfer of address/data/control information, was described. (A10501(5:22-25).) As discussed above, the clocking scheme was described as a separate inventive concept from the interface to the new multiplexed address/data/control bus. *See* A10501(5:19-20) and A10502(6:13-15).)

Another important discussion distinguishing the prior art is found in the Detailed Description section, where the applicants explain that the separate address,

data, and control lines used in the prior art are replaced with the invention's multiplexed bus lines:

> There is no need for separate device-select lines since device-select information for each device on the bus is carried over the bus. There is no need for separate address and data lines because address and data information can be sent over the same lines.

(A10508(12:2-6).)

Finally, near the end of the specification, the applicants concede that many of the disclosed features had been used in the prior art, "but never in conjunction with *the bus architecture of this invention*." (A10555(59:23-25)(emphasis added).) These consistent descriptions of the prior art and how the "invention" differed from the prior art demonstrate that the invention described in the '898 application required an interface to a narrow multiplexed bus.

Because claims 26 and 28 do not limit the way in which the recited memory device communicates with the rest of the system and are not limited to the "multiplexed bus" as described in the '898 patent, claims 26 and 28 do not have written description support in the '898 application. As a result, Rambus cannot claim priority to the '898 application, JEDEC and Park are prior art, and the Board erred in not applying those references against claims 26 and 28.

VI. CONCLUSION

As demonstrated above, substantial evidence supports the Board's factual findings that claims 26 and 28 of the '916 Patent are anticipated by Bennett. Therefore, Micron respectfully requests that this Court affirm the Board's decision that claims 26 and 28 are anticipated.

Alternatively, Micron respectfully requests that this Court reverse the Board's determination that claims 26 and 28 of the '916 Patent are entitled to the benefit of the earlier filing date and remand to the Board for consideration of JEDEC and Park as anticipating references.

Dated: July 19, 2013

Respectfully submitted,

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United States Court of Appeals
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RAMBUS, INC. v MICRON TECHNOLOGY, INC., 2013-1192

CERTIFICATE OF SERVICE

I, Henry A. Petri, Jr. being duly sworn according to law and being over the age of 18, upon my oath depose and say that:

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July 19, 2013

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